IN THE CLAIMS:

No claims have been amended herein. Claims 13-18 have been added. All of the pending claims 1, 2, and 13-18 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Original) A method for electrically testing a flip-chip semiconductor assembly formed from at least one integrated circuit (IC) die and a substrate, the method comprising:
contacting the substrate with probes;
while the substrate is in contact with the probes, bringing the at least one die and the substrate together in conductive contact to form the flip-chip semiconductor assembly; and
before the at least one die is sealed, electrically testing the assembly using the probes.

2. (Previously Presented) The method of claim 1, wherein contacting the substrate with the probes comprises contacting the substrate with the probes at a die-attach station.

3. (Withdrawn) A method for in-line electrical testing of a flip-chip semiconductor assembly during its manufacture, the method comprising:
providing one or more integrated circuit (IC) dice, each with a surface having interconnection bumps thereon;
providing a printed circuit board (PCB) with conductive epoxy pads deposited on a surface thereof for flip-chip attachment to the interconnection bumps of the one or more IC dice;
providing an in-line electrical test socket for connection to the PCB;
inserting the PCB into the test socket;
positioning the one or more IC dice on the surface of the PCB with the interconnection bumps of the one or more dice in conductive contact with the epoxy pads of the PCB to form the flip-chip semiconductor assembly;
attaching the one or more IC dice to the PCB;
while the PCB is inserted in the test socket and before encapsulation of the one or more IC dice,

electrically testing the assembly using the test socket;
repairing the assembly if it fails the electrical testing; and
encapsulating the one or more IC dice of the assembly.

4. (Withdrawn) A method for in-line electrical testing of a flip-chip semiconductor assembly during its manufacture, the method comprising:
providing one or more integrated circuit (IC) dice, each with a surface having interconnection bumps thereon;
providing a substrate with conductive quick-cure epoxy pads deposited on a surface thereof for flip-chip attachment to the interconnection bumps of the one or more IC dice;
providing an in-line electrical test socket for connection to the substrate;
inserting the substrate into the test socket;
positioning the one or more IC dice on the surface of the substrate and pressing the interconnection bumps of the one or more dice into conductive contact with the epoxy pads of the substrate to form the flip-chip semiconductor assembly;
attaching the one or more IC dice to the substrate;
while the substrate is inserted into the test socket and before sealing of the one or more IC dice, electrically testing the assembly using the test socket;
repairing the assembly if it fails the electrical testing;
curing the quick-cure conductive epoxy pads of the substrate; and
sealing the one or more IC dice of the assembly.

5. (Withdrawn) A method for electrically testing a flip-chip semiconductor assembly during its manufacture, the assembly being formed from a substrate and one or more integrated circuit (IC) dice, the method comprising:
connecting the substrate to a test apparatus at a die-attach station;
bringing the one or more IC dice into a flip-chip-type conductive contact with the substrate while the substrate is connected to the test apparatus at the die-attach station to form the flip-chip semiconductor assembly; and
electrically testing the assembly at the die-attach station using the test apparatus.

6. (Withdrawn) The method of claim 5, wherein bringing the one or more IC dice into a flip-chip-type conductive contact with the substrate comprises pressing the one or more IC dice against a surface of the substrate so interconnection bumps on the one or more dice are in conductive contact with conductive pads on the surface of the substrate.

7. (Withdrawn) The method of claim 5, wherein bringing the one or more IC dice into a flip-chip-type conductive contact with the substrate comprises flip-chip-attaching the one or more IC dice to the substrate.

8. (Withdrawn) A method for electrically testing a flip-chip semiconductor assembly formed from at least one integrated circuit (IC) die and a substrate, the method comprising:

inserting the substrate into a test socket;

while the substrate is in the test socket, bringing the at least one die and the substrate together in conductive contact to form the flip-chip semiconductor assembly; and

before the at least one die is sealed, electrically testing the assembly using the test socket.

9. (Withdrawn) A method for in situ electrical testing of a flip-chip semiconductor assembly during its manufacture, the method comprising:

providing one or more integrated circuit (IC) dice, each with a surface having interconnection bumps thereon;

providing a substrate with conductive pads deposited on a surface thereof for flip-chip attachment to the interconnection bumps of the one or more IC dice;

providing an in situ electrical test socket for connection to the substrate;

inserting the substrate into the test socket;

positioning the one or more IC dice on the surface of the substrate with the interconnection bumps of the one or more dice in conductive contact with the pads of the substrate to form the flip-chip semiconductor assembly;

while the substrate is inserted into the test socket and the one or more IC dice are positioned on

the surface of the substrate, and before sealing of the one or more IC dice, electrically testing the assembly using the test socket;

repairing the assembly if it fails the electrical testing; and

sealing the one or more IC dice of the assembly.

10. (Withdrawn) A method for in situ electrical testing of a flip-chip semiconductor assembly during its manufacture, the method comprising:

providing one or more integrated circuit (IC) dice, each with a surface having interconnection bumps thereon;

providing a printed circuit board (PCB) with conductive epoxy pads deposited on a surface thereof for flip-chip attachment to the interconnection bumps of the one or more IC dice;

providing an in situ electrical test socket for connection to the PCB;

inserting the PCB into the test socket;

positioning the one or more IC dice on the surface of the PCB with the interconnection bumps of the one or more dice in conductive contact with the epoxy pads of the PCB to form the flip-chip semiconductor assembly;

while the PCB is inserted in the test socket and the one or more IC dice are positioned on the surface of the PCB, and before encapsulation of the one or more IC dice, electrically testing the assembly using the test socket;

repairing the assembly if it fails the electrical testing; and

encapsulating the one or more IC dice of the assembly.

11. (Withdrawn) A method for in situ electrical testing of a flip-chip semiconductor assembly during its manufacture, the method comprising:

providing one or more integrated circuit (IC) dice, each with a surface having interconnection bumps thereon;

providing a substrate with conductive quick-cure epoxy pads deposited on a surface thereof for flip-chip attachment to the interconnection bumps of the one or more IC dice;

providing an in situ electrical test socket for connection to the substrate;

inserting the substrate into the test socket;

positioning the one or more IC dice on the surface of the substrate and pressing the interconnection bumps of the one or more dice into conductive contact with the epoxy pads of the substrate to form the flip-chip semiconductor assembly;

while the substrate is inserted into the test socket and the one or more IC dice are positioned on the surface of the substrate, and before sealing of the one or more IC dice, electrically testing the assembly using the test socket;

repairing the assembly if it fails the electrical testing;

curing the quick-cure conductive epoxy pads of the substrate; and

sealing the one or more IC dice of the assembly.

12. (Withdrawn) A method for in situ electrical testing of a flip-chip semiconductor assembly during its manufacture, the method comprising:

providing one or more integrated circuit (IC) dice, each with a surface having interconnection bumps thereon;

providing a substrate with conductive epoxy pads deposited on a surface thereof for flip-chip attachment to the interconnection bumps of the one or more IC dice;

providing an in situ electrical test socket for connection to the substrate;

inserting the substrate into the test socket;

positioning the one or more IC dice on the surface of the substrate with the interconnection bumps of the one or more dice in conductive contact with the epoxy pads of the substrate to form the flip-chip semiconductor assembly;

curing the conductive epoxy pads of the substrate;

while the substrate is inserted into the test socket and the one or more IC dice are positioned on the surface of the substrate, and before sealing of the one or more IC dice, electrically testing the assembly using the test socket;

repairing the assembly if it fails the electrical testing; and

sealing the one or more IC dice of the assembly.

13. (New) The method of claim 1, wherein the act of bringing the at least one IC die and the substrate together comprises pressing the at least one IC die against a surface of the substrate so bond pads on a surface of the at least one IC die are in a curable conductive contact with conductive pads on the surface of the substrate.

14. (New) The method of claim 23, further comprising placing conductive epoxy dots on one of the bond pads on the at least one IC die and the conductive pads on the substrate.

15. (New) The method of claim 24, wherein the conductive epoxy dots comprise one of dry conductive epoxy dots and wet conductive epoxy dots.

16. (New) The method of claim 1, wherein the act of bringing the at least one IC die and the substrate together comprises flip-chip attaching the at least one IC die to the substrate.

17. (New) The method of claim 1, further comprising reworking the flip-chip semiconductor assembly and retesting the flip-chip semiconductor assembly if the flip-chip semiconductor assembly fails the electrical testing act.

18. (New) The method of claim 1, further comprising curing the curable conductive contact if the flip-chip semiconductor assembly passes the electrical testing act.